



RVfpga: Complete Courses in Computer Architecture & SoC Design

RVfpga has been created to provide the foundation knowledge and hands-on experience that the next generation of Programmers and Engineers need to harness the potential of RISC-V. It is structured for Teachers to use with their Students, but can also be used for self-study. Supporting videos, workshops and online courses are available now and in further development. It is suitable for under-graduate students, and is also useful to post-grads for self-study, as well as industry professionals who want to update their skills. It's rigorous, providing everything a Teacher needs: how to set-up the course, the hardware and software tools, lecture slides, student manuals and supplementary materials. Even suggested exam questions!

In total these materials would typically fit into three semesters, making RVfpga by far the most complete set of materials on these topics. Furthermore, they are available in seven languages: English, Simplified Chinese, Traditional Chinese, Japanese, Korean, Spanish & Turkish.

BY ACADEMICS FOR ACADEMICS

We follow the essential principle 'by academics for academics' in the creation of all teaching materials. RVfpga is a collaborative effort between Imagination Technologies' University Programme ("IUP"), UNLV – University of Nevada Las Vegas and UCM – Complutense University of Madrid. Our curriculum guides and reviewers are from UCB – University of California, Berkeley, PDX – Portland State University, and ZJU - Zhejiang University.

The RVfpga package consists of 20 Labs in total with detailed instructions, examples, short questions and practical exercises with solutions, giving teachers flexibility to choose between a practical and an exam-based structure for the course.

The materials are provided in both .pdf and .pptx/.docx formats enabling customisation by Teachers to suit their needs.

"RVfpga: Understanding Computer Architecture" instructions, tools, and labs show how to:

- Target a commercial RISC-V system to an FPGA and a Simulator
- Program the core using C and RISC-V assembly languages
- Use the peripherals from the RVfpga System and add new peripherals
- Analyse and modify the RISC-V core and memory hierarchy
- A total of two semesters of materials at typical teaching pace

"RVfpga-SoC: An Introduction to SoC Design" enables users to gain hands-on experience, understand, and walk through the process of building a System-on-Chip. RVfpga-SoC guides users through the interconnect options and adding peripherals.

It then shows how to run a real-time operating system ("RTOS") and run a program using Tensorflow Lite on the SweRVolf core.



The RVfpga system uses Chips Alliance's SweRVolf SoC, based on Western Digital's RISC-V SweRV EH1 core. The SweRV is a fully-verified production level processor core. It is fully open-source, and is now being used by several companies in silicon, including by Western Digital in data storage and Imagination Technologies in their latest GPUs (A, B and C series).

SweRV is at the centre of a vibrant expanding ecosystem with many useful open-source and commercial tools available, including Simulators, Models, Integrated Development Environments, Virtual Hardware and pre-configured FPGA-ready SoC implementations. We believe passionately in sharing real-world in-silicon solutions with Students. Why use a "simplified education core" when you can use industrially proven designs?

COURSE CONTENT

Semesters 1&2: "RVfpga: Understanding Computer Architecture!"

0. RVfpga Labs Overview
1. Creating a Vivado Project
2. C Programming
3. RISC-V Assembly Language
4. Function Calls
5. Image Processing: Projects with C & Assembly
6. Introduction to I/O
7. 7-Segment Displays
8. Timers
9. Interrupt-Driven I/O
10. Serial Buses
11. SweRV EH1 Configuration and Organization. Performance Monitoring
12. Arithmetic/Logical Instructions: the add instruction
13. Memory Instructions: the lw and sw instructions
14. Structural Hazards
15. Data Hazards
16. Control Hazards. Branch Instructions: the beq Instruction. The Branch Predictor.
17. Superscalar Execution
18. Adding New Features (Instructions, Hardware Counters) to the Core
19. Memory Hierarchy. The Instruction Cache.
20. ICCM and DCCM

Semester 3: "RVfpga-SoC: Introduction to SoC Design"

1. Introduction to RVfpga-SoC
2. Running Software on the RVfpga SoC
3. Introduction to SweRVolf and FuseSoC
4. Building and Running Zephyr on the SweRVolf
5. Running Tensorflow Lite on SweRVolf

PROJECTS for 2022

- *One Day Workshop series in Universities and online videos
- *Online courses on EdX in English and iCourse in Chinese using the new "VDB" - Virtual Development Board
- *New Labs and supplementary materials
- *The latest RISC-V Edition of the widely-used textbook "Digital Design & Computer Architecture" by Sarah Harris & David M. Harris is a uniquely useful complement to RVfpga



GETTING THE MATERIALS

They are completely free-of-charge for academic and training use.

Register for the “IUP” – Imagination University Programme: <https://university.imgtec.com/register>

Request the materials: <https://university.imgtec.com/teaching-download/>

MORE INFORMATION:

[IUP Brochure](#)

[HOW TO REGISTER](#)