Join us in the classroom!
Put RISC-V into your Computer Architecture course using RVfpga!

Dear Professors and Friends,
Online is convenient and it has saved us during the pandemic, but you can't beat in-person, in-class! That immersive feeling of hands-on and the shared mission with colleagues all trying to master the same subject.

We are at the start of a global series of workshops to "train the teachers" how to use RISC-V in computer architecture courses and the design of systems on chip (SoCs).
We are starting in the USA, then in Europe and then across Asia.
Our RVfpga partners, including Digi-Key are working with us to make this possible!

To do this, we are asking for a day of your time so that you can empower the next generation of computer science and engineering students to get real-world expertise in computer architecture and the RISC-V instruction set architecture.

What is RVfpga about?
This RVfpga workshop presents a commercial RISC-V system targeted to an FPGA, discusses the theory, architecture, and course structure, and shows how to use the hands-on labs as part of the complete RVfpga course. The course explores the fundamentals of computer architecture using Western Digital's open-source, fully verified, already in-silicon, SweRV EH1 RISC-V core targeted to a Xilinx Artix 7 FPGA on Digilent's Nexys A7 development board. Everyone will get hands-on experience with the FPGA platform and the software tools, enabling a fast start when you return to your university.
The SweRV is not an "education core" it's real-world, used inside Imagination's GPUs and Western Digital's solid-state drives.

What will you learn?
- The workshop shows how to quickly get the RISC-V FPGA system and RISC-V tools up and running.
- We describe each of the labs and work through a selection of them hands-on.

- We will also discuss how to integrate RVfpga into your curriculum.

Specific topics include:
• Installing the tools (which we encourage before the workshop)
• Targeting the SweRV EH1 RISC-V core and SoC to an FPGA
• Programming the RISC-V SoC
• Adding more functionality to the RISC-V SoC
• Analyzing and modifying the RISC-V-core and memory hierarchy

Who should attend?
- It's primarily a "Train the **Teacher**" event, of greatest value to EE, CS and CE Teachers who want to teach Computer Architecture.
- **Trainers** in commercial companies and postgrads who are considering a career in teaching, or becoming a chip designer will also find it useful.

Networking
It's a great opportunity to make new and refresh existing links to fellow Professors who are keen to keep their courses up-to-date. Help us spread the word and bring your colleagues.

Our Trainers:
USA
Dr. Sarah Harris, professor of electrical and computer engineering at the University of Nevada, Las Vegas. Sarah Harris earned her M.S. and Ph.D. at Stanford University. She is the co-author of three popular textbooks: Digital Design and Computer Architecture, 2nd Edition (2007), ARM Edition (2015), and RISC-V Edition (2021). Her research interests include computer architecture and applications of embedded systems and machine learning to biomedical engineering and robotics.
Europe
Daniel A. Chaver Martínez obtained a Physics Degree from University of Santiago de Compostela (USC) in 1998 and an Electronic Engineering Degree from University Complutense of Madrid (UCM) in 2000. He developed his PhD from 2000 to 2006 at UCM. He has taught many different courses related to Computer Architecture since 2000. His current research interests include: Architectural Techniques for the Cache and for Non-volatile Memories and OS Scheduling for Asymmetric MultiProcessors. Since 2015, he has been collaborating with Imagination Technologies in the development of processors and teaching materials.

First Workshop Location:
The University of Nevada, Las Vegas
4505 S. Maryland Parkway
Las Vegas, Nevada 89154
- 20 minutes by Uber from Las Vegas airport (LAS)

Dates
Each workshop runs for one-day, and there are two consecutive dates, Friday May 20th and Saturday May 21st. Please register below for your preferred date.
The links are in the table below.

RVfpga EVENTS & WORKSHOPS

DATE	LOCATION/EVENT	CITY, COUNTRY	FORMAT	Registration
May 3rd to 5th	**CICSU**	**Paris, France**	**RISC-V Week: Poster**	**Via event**
		https://open-src-soc.org/2022-05/registration.html [open-src-soc.org]		
May 20th & 21st	**UNLV**	**Las Vegas, Nv, USA**	**TWO RVfpga Workshops**	**See above**
		https://www.eventbrite.co.uk/e/rvfpga-risc-v-fpga-understanding-computer-architecture-workshop-may-20th-tickets-302656422507 [eventbrite.co.uk]		
		https://www.eventbrite.co.uk/e/rvfpga-risc-v-fpga-understanding-computer-architecture-workshop-may-21st-tickets-302842930357 [eventbrite.co.uk]		
June 22nd	**HiPEAC**	**Budapest, Hungary**	**RVfpga Workshop**	**Via event**
		https://www.hipeac.net/2022/budapest/#/ [hipeac.net]		
July 4th & 5th	**Imperial College**	**London, UK**	**TWO RVfpga Workshops**	**Eventbrite**
		https://www.eventbrite.co.uk/e/risc-v-fpga-understanding-computer-architecture-workshop-july-4th5th-tickets-318697551957		
August To be confirmed	**TBC**	**Eastern USA**	**TWO RVfpga Workshops**	**Eventbrite TBC**
September To be confirmed	**Rice University**	**Houston, Tx, USA**	**RVfpga Workshop**	**Eventbrite TBC**
September 7th & 8th	**HMUAS University of Applied Sciences**	**Munich, Germany**	**TWO RVfpga Workshops**	**Eventbrite**
		https://www.eventbrite.co.uk/e/risc-v-fpga-understanding-computer-architecture-workshop-sep-7th8th-tickets-318709216847		
September 20th (Before SARTECO)	**University of Alicante**	**EPS Department, Alicante, Spain**	**RVfpga Workshop**	**Eventbrite**
		https://www.eventbrite.co.uk/e/risc-v-fpga-understanding-computer-architecture-workshop-sep-20th-tickets-316486187707		
Q4'22/Q1'23 To be confirmed	**ZJU Hangzhou, RIOS Shenzhen, Beijing + TBC**	**China**	**TWO RVfpga Workshops at each location**	**TBC**
2023	**TBC**	**Taiwan, Korea, Japan**		**TBC**

More information

- About the IUP and RVfpga: https://university.imgtec.com/teaching-download/

- RISC-V blog: https://blog.imaginationtech.com/how-rvfpga-understanding-computer-architecture-will-give-under-grads-real-world-skills

We look forward to meeting you in-person!

Best Regards,

Robert C.W. Owen
Principal Consultant: Worldwide University Programme
Imagination